QuadTech

Application Note

The Application of Digital Signal Processing (DSP) Techniques to Precision LCR Measurements

Existing automatic LCR meters use analog techniques to detect the in-phase and quadrature components of the unknown's (DUT's) impedance. This information is then used to calculate other parameters of interest (R, L, C, Q etc.) The problem with these analog techniques is that they suffer from slow throughput and limited bandwidth. Digital techniques, adapted from the signal processing disciplines, offer the promise of high precision accompanied by high-speed measurement capability. The high demand for this technology generated by video and telecommunications industries offers the additional advantage of low cost. While some existing designs offer digitally generated stimulus signals, the frequency selection has been less than adequate for today's complex passive component testing needs. The use of Direct Digital Synthesis (DDS) of the test signal results in very high frequency resolution across the available frequency spectrum.

Basic Techniques

Early commercial LCR "bridges" used a variety of techniques involving the matching or "nulling" of two signals derived from a single source. The first signal generated by applying the test signal to the unknown and the second signal generated by utilizing a combination of known-value R and C standards. The signals were summed through a detector (normally a panel meter with or without some level of amplification). When zero current was noted, it could be assumed that the current magnitude through the unknown was equal to that of the standard and that the phase was exactly the reverse (180° apart). The combination of standards selected could be arranged to read out C and D_F directly as in the QuadTech Model 1620 and 1621 Capacitance Bridges. Automatic bridges have generally not used the nulling technique but rely on a combination of microprocessor control and phase sensitive detectors.

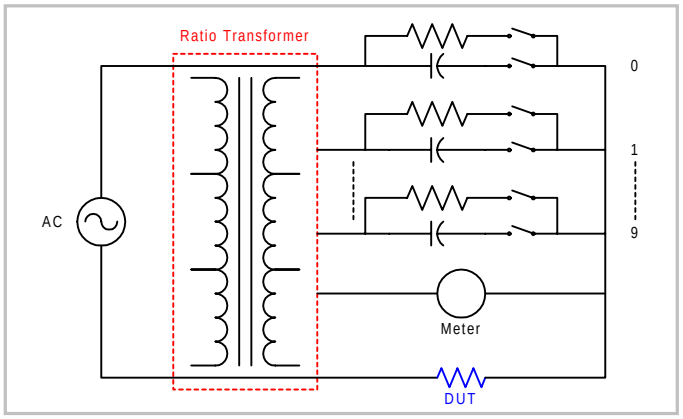

Figure 1: Ratio Transformer Method of Null Detection

The Phase Sensitive Detector

The balanced bridge detector is not well suited to automation due to the many sensitive nodes that must be switched to achieve a null. In the late 1970s H.P. Hall of GenRad Instruments introduced his design of a synchronous detector circuit to solve this problem. Mr. Hall's synchronous detector invention was granted U.S. Patent # 4,181,949.

Whereas the null detector uses a combination of precisely known standards, the synchronous detector utilizes a single (reference) resistor (R_S) of relatively low accuracy. The detector operates by gathering either the in-phase or quadrature component of the current through the unknown. This is accomplished by multiplying the current by the sine of the stimulus for the in-phase component or the cosine for the quadrature.

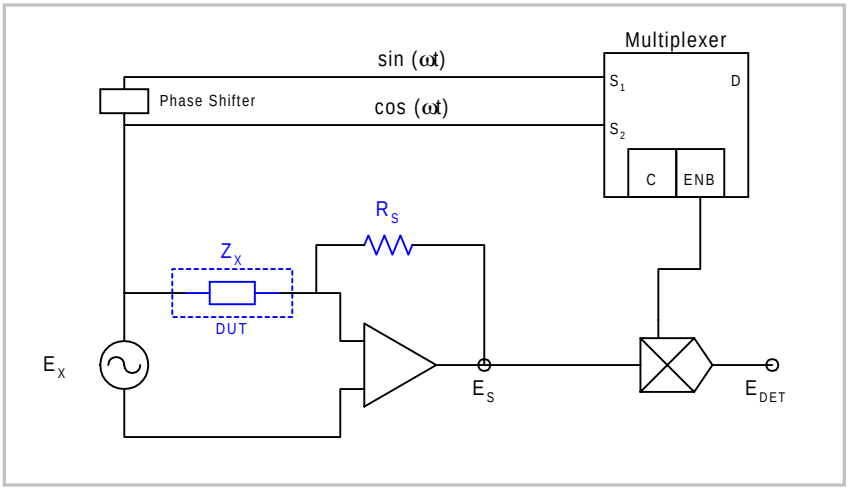

Figure 2: Basic Synchronous Detector Circuit

Depending upon which input to the multiplexer is selected, the detector voltage, E_{DET}, will represent E_S [sin (ωt)] or E_S [cos (ωt)]. Since the voltage applied is known, the admittance of the DUT, as a complex vector, can be calculated. $Z_X = R_S (E_X/E_S)$. From the admittance, any desired parameter may be calculated.

In order for the technique to be effective, the arithmetic requires that:

1. The current representation, Es, and the sine wave being multiplied are synchronous to the stimulation signal Ex. Any phase relationship between the signals is acceptable as long as it is constant throughout the detection time.

2. The multiplication is performed over an integer number of cycles.

Implementation Difficulties

The technique of choice for multiplying the two signals has been to use a multiplying D/A converter. The signal, Es, is applied to the reference input of the D/A and a series of binary numbers representing a sine or cosine wave are applied to the digital input. In order to achieve synchronization, the sine wave stimulus is generated by applying the identical binary stream to a second D/A.

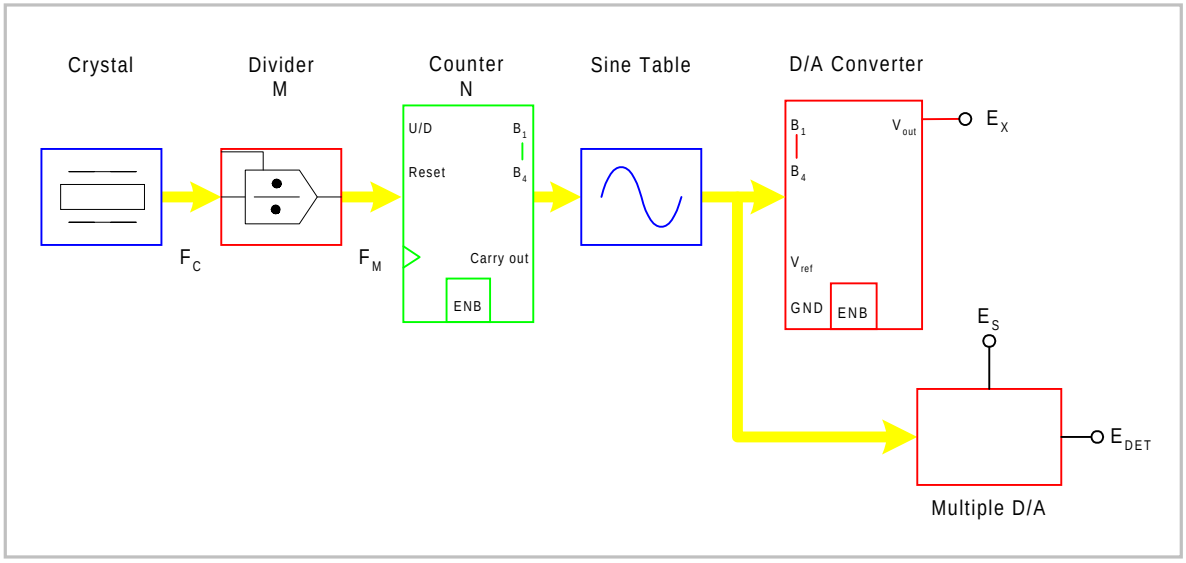

Figure 3: Digital Sine Wave Generation and Synchronous Detection

The method of using the same binary stream to drive both D/A's simultaneously assures perfect synchronization. This implementation has worked well providing flexible, automatic measurement capability with a high degree of precision and speed. It has two factors that have limited its effectiveness: the bandwidth of the multiplying D/A, and the ability of the source to generate frequencies with a high degree of resolution. Multiplying four quadrant D/A's with bandwidth above a few hundred kilohertz is simply not available at reasonable cost.

The frequency generation scheme provides synchronization by using a ROM look-up table to drive both D/A's. A binary counter that repeatedly counts from 0 to N drives this ROM look-up table. N is the size of the look-up table and is typically in the range of 64-1024. The frequency of the sine wave is $F_C/(M \bullet N)$. The difficulty is that the division is integer, and not all frequencies can be produced.

For a sine table of size 256, and a crystal frequency of 38.6 MHz, the following may be produced:

M=1	f=150 kHz
M=2	f=75 kHz
M=3	f=50 kHz

As can be inferred from the above example, no combination of crystal frequency and N will produce all desired frequencies in a general-purpose meter. If one is willing to reduce the number of "sample points" from the look-up ROM (resulting in more noise) the value of N can be adjusted in concert with M to provide additional values. In practice there has always been a large number of desirable values of f which can only be approximated.

Direct Digital Synthesis

The Direct Digital Synthesis (DDS) approach has been used for some time to generate sine waves for test and measurement purposes. A variety of commonly available equipment, such as arbitrary waveform generators and modems utilize DDS in integrated circuit form to great advantage.

The DDS is a variation of the Sine ROM look-up that provides very high resolution of the generated frequency, Fg. Like the counter driven look-up, a DDS provides phase information to a Sine ROM table to drive a D/A. Whereas the counter provides the identical phase numbers over and over to the ROM (0-N), a DDS varies the phase points from cycle to cycle to provide a higher resolution. The counter always returns to phase "zero" at the beginning of each cycle, the DDS does not necessarily do so.

To create a specific frequency, the DDS is loaded with a phase increment, a digital word of high precision (typically 32 bits) that is a representation of the step size between ROM table look-ups. This phase increment is continuously added to a phase accumulator whose output is applied to the sine look-up table. The sine look-up table is normally of considerably less precision than the accumulator (say 16 bits). The look-up results are then truncated to 8, 10, or 12 bits and applied to a D/A for generation of the sine wave. The frequency (Fg) generated by a 32-bit accumulator running at 30MHz is:

$$Fg = \frac{Fs \times \Delta\Phi}{2^n} = \frac{30 \times 10^6 \times \Delta\Phi}{2^{32}}$$

The phase increment is not necessarily an even multiple of 2π. This being the case, on completion of the first cycle the phase accumulator would not return to zero but would start the next cycle at some point beyond zero degrees. Typical commercially available IC's are capable of producing sine waves from 1Hz to 20MHz with .004Hz resolution. The resolution available with a 32-bit accumulator clocked at 30MHz is:

$$R = \frac{Fs}{2^{32}} = \frac{30 \times 10^6}{2^{32}} = 0.00698 Hz$$

From these numbers we see that extremely fine resolution may be obtained.

Digital Sampling

In order to overcome the bandwidth limitations of multiplying D/A's, a number of investigations have been launched using digital sampling techniques to analyze the current signal through the unknown. A representative implementation is illustrated in Figure 4.

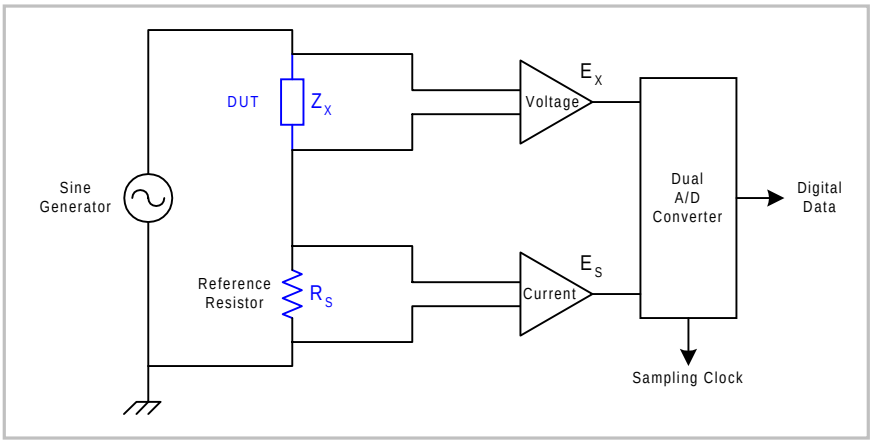

Figure 4: Digital Detector Circuit

The voltage across the standard (reference) resistor Rs is applied to an A/D converter that takes samples during one or more integer cycles of the stimulus sine wave. The number of samples, N, per sine wave is usually a power of 2 in the range 64 to 1024. The voltage across the unknown is also sampled at the same rate and time. When the samples from each of the two channels are collected, they are multiplied mathematically by the sine and cosine of the appropriate angle by a microprocessor. Due to speed considerations, it is common to utilize a DSP. This algorithm results in obtaining the real and imaginary parts of the two voltages. The admittance of the unknown can then be calculated. $Z_X = R_S (E_X/E_S)$.

While the digital technique eliminates the multiplying D/A, it replaces it with an A/D converter that must be able to sample the waveform at N times the sine wave frequency. For N=64 and a test frequency of 1MHz, this requires a sampling A/D with a rate of 64MHz! Fortunately this requirement may be overcome by using a technique known as under sampling.
In under sampling, the A/D converter still takes the same number of samples of the signal, but it does so over multiple cycles.

For example: four samples are needed from a test signal of 1MHz (1µsec period), and the A/D can only sample at 100kHz (10µsec period). The first sample is taken at the beginning of the first cycle (0°) then the second is not taken until ten cycles have passed (10 • 1µsec = 10µsec). At this point the wave would be sampled at 90° and the third sample 10 cycles later at 180°. The last 10 cycles after that at 270°. Thus a total of 30 cycles of the stimulus is required to fetch all the data.

A Few More Words on Digital Sampling

The one factor that can not be ignored when taking digital samples is that the sample timing must be exactly synchronous to the sine wave. Put another way, the digital sampling clock must be exactly N times the sine wave frequency and locked to it. The phase difference between the two must not vary during the sample time.

For a sine wave generator using a binary divide with a look-up table, this is not a problem. The same clock that drives the counter can be used to control the sampling.

Synchronizing the DDS

The difficulty with using a DDS for the sine wave generation has been that there was no way to synchronize the sampling detector to it. The crystal driving the DDS may be available, but there has been no way to use this to come up with an exact multiple of the sine wave being generated according to how many samples are being taken. This problem can be overcome by using a second DDS. The two DDS circuits, driven by the same crystal, run at multiples of the same frequency. The MSB of the second DDS is used as a clock to drive the sampling circuit. This clock is now totally synchronous to the internal digital workings of the sine wave DDS.

For example, if a 1kHz stimulus were desired, DDS #1 could be set up to produce a 1kHz sine look up. If it were desired to take 1024 samples during the sine wave, the second DDS would be set up for 1024 •1kHz or 1.024MHz. The MSB of the digital word that would normally drive a Sine ROM is instead used to produce a digital clock to drive the sampling circuits. The digital sampling timer now knows that there will be precisely 1024 sample clocks per sine wave cycle. Neither the sampling circuit nor the second DDS have any idea when the sine wave stimulus "starts" (when zero crossing occurs). This is not necessary to perform the FFT algorithm. What is known is that, whatever the phase relationship, it is constant throughout the sampling period.

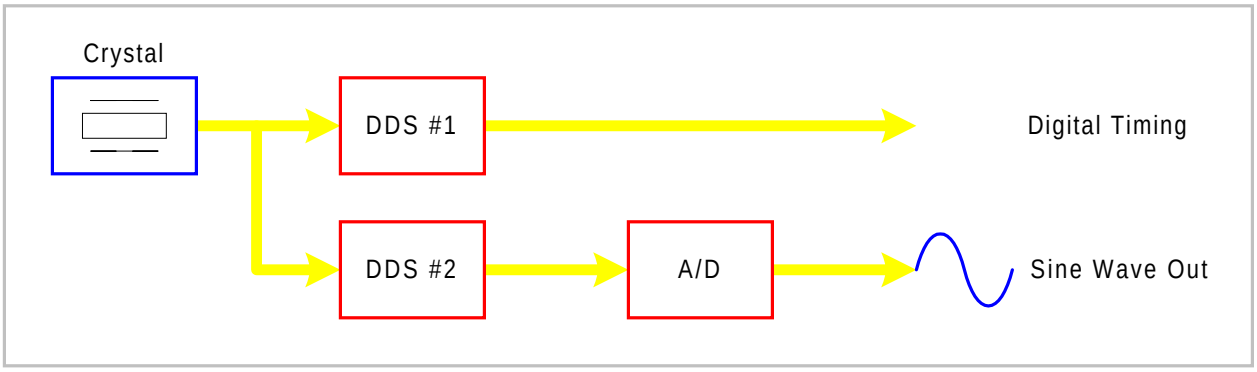

Figure 5: Dual DDS Synchronization

In practice, DDS circuits are offered in pairs on a single IC. This is cost-effective and provides better coherence between the two DDS's due to their being on the same die.

Results

QuadTech has utilized the described methods of digital sampling and DDS generation of the sine wave in the 7000 Series Precision LCR Meters. The DDS pair employed in the 7000 Series instrument generates sine waves from 10Hz to 500kHz. The resolution available is 0.1Hz from 10Hz to 10kHz, and five digits of resolution above 10kHz. The circuit design was done quite conservatively and there is every reason to believe that this resolution may be increased in the future.

The sampling circuit of the 7000 Series instrument utilizes two fast 'sample-and-hold' IC's in front of a dual 18-bit Analog to Digital converter. The sampling rate is a maximum of 80kHz. The under sampling technique is working well up through the range of frequencies. The combination of DDS and sampling detector is providing 0.05% accuracy on primary parameters (R, L, C) and 500ppm on secondary parameters such as D_F and Q. The units were designed as bench top analyzers with speed as a secondary consideration, but in FAST mode will measure at 40 measurements per second.

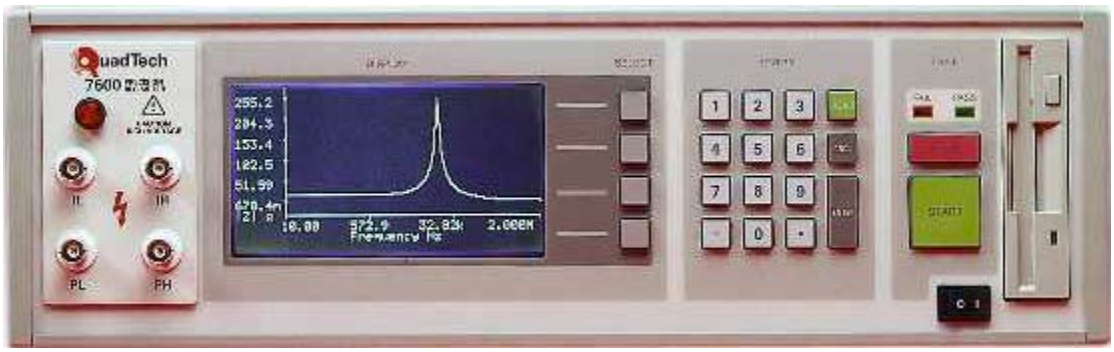

Figure 6: QuadTech 7000 Series Precision LCR Meter

Conclusion

Superior performance in frequency resolution, speed and accuracy over wide frequency ranges may be gained by use of Digital Signal Processing techniques. These techniques are easily achievable with common off-the-shelf IC's at relatively low cost. The application of these techniques has only begun to be investigated and should continue to yield advances in the state-of-the-art of LCR measurement over the next several years.

For complete product specifications on the 7000 Series Precision LCR meters or any of QuadTech's products, visit us at http://www.quadtech.com/products. Call us at 1-800-253-1230 or email your questions to info@quadtech.com.

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